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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,130	10/29/2003	James Joseph Chambers	TI-36030	7267

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,130	CHAMBERS, JAMES JOSEPH	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *13-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 9-12* is/are rejected.

7)☒ Claim(s) *3-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Election dated February 17, 2005, Applicant has elected invention of Group I (claims **1-12)** without traverse is acknowledged. Accordingly, claims **13-29** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims **13-29**, drawn to a semiconductor device.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 10/29/03. The references cited on the PTOL 1449 form have been considered.

Specification

The disclosure is objected to because of the following informalities:

The disclosure is objected to because of the following informalities: The related application information on page 1 should be updated.

On page 3, lines 4, 6, 7 and 13, "Fig. 10A and Fig. 10B" should read –Fig. 11A and Fig. 11B--.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-2 and 9-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (USP 6,064,107 hereinafter referred to as "Yeh") in view of Dixit et al. (US 2005/0051812 A1 hereinafter referred to as "Dixit").

Regarding claims **1 and 2**, Yeh discloses in Figs. 2A-2E and the corresponding texts as set forth in column 2, line 65-column 3, line 65, a method of fabricating a semiconductor transistor, the method comprises:

creating a form structure 110 above a starting structure 100, the form structure having an opening exposing a single portion of the starting structure;

forming a spacer 104 in the opening of the form structure, the spacer extending over part of the starting structure along a sidewall of the form structure opening;

forming a semiconductor material 106 in the opening of the form structure to create a formed semiconductor body 106 having a single generally planar bottom surface above the starting structure; and

removing the form structure and the spacer.

Yeh fails to teach the method comprises the step of removing the spacer, forming a gate structure disposed along at least a portion of a top and sides of the formed semiconductor body, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the formed semiconductor body; and doping portions of the formed semiconductor body to form source/drains, wherein the formed semiconductor body comprises a first body portion, a second body portion, and a third body portion, the second body portion being disposed between the first and third body portions and having first and second sides and a top, and wherein the gate structure is formed along at least a portion of the top and sides of the second body portion.

Dixit teaches in Figs. 1a-1b and the corresponding texts as set froth in paragraphs [0026]-[0028] that a method for manufacturing a FinFET comprises forming a gate structure 107 disposed along at least a portion of a top and sides of the formed semiconductor body 102, 106, the gate structure comprising a conductive gate electrode 107a and a gate dielectric 107b disposed between the gate electrode and the formed semiconductor body; and doping portions of the formed semiconductor body to form source/drains 102, 104, 105, wherein the formed semiconductor body comprises a first body portion, a second body portion, and a third body portion, the second body portion being disposed between the first and third body portions and

having first and second sides and a top, and wherein the gate structure is formed along at least a portion of the top and sides of the second body portion.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of forming a gate structure disposed along at least a portion of a top and sides of the formed semiconductor body, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the formed semiconductor body; and doping portions of the formed semiconductor body to form source/drains, wherein the formed semiconductor body comprises a first body portion, a second body portion, and a third body portion, the second body portion being disposed between the first and third body portions and having first and second sides and a top, and wherein the gate structure is formed along at least a portion of the top and sides of the second body portion, as taught by Dixit to incorporate into Yeh's teachings to form the semiconductor body with the gate structure disposed along the semiconductor body in order to achieve a multiple gate semiconductor device.

Regarding claims **9-11**, Yeh discloses in Figs. 2A-2E the method wherein forming the spacer comprises depositing a spacer material layer over the form structure and over the exposed starting structure; and etching the spacer material layer to expose a portion of the starting structure, leaving a portion of the spacer material layer extending over part of the starting structure along the sidewall of the form structure opening, wherein depositing the spacer material layer comprises depositing silicon nitride over the form structure and over the exposed starting structure, and wherein removing the form structure and the spacer comprises wet etching the

form structure and the spacer, leaving the formed semiconductor body having a single generally planar bottom surface above the starting structure.

Regarding claim **12**, Yeh discloses all the claimed limitations except for the spacer material layer is deposited using chemical vapor deposition or atomic layer deposition. Dixit teaches that various techniques exist in semiconductor technology to deposit layer, for example, one such technique is chemical vapor deposition (CVD). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use CVD to deposit the spacer material layer since it was known in the art that chemical vapor deposition (CVD) includes a wide range of deposition processes such as epitaxial growth, atomic layer CVD and plasma enhanced CVD (see Dixit, paragraph [0050]).

Allowable Subject Matter

Claims **3-8** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. The prior art of record fails to teach or render obvious the method wherein forming the spacer comprises depositing a second spacer material layer over the first spacer material layer; and etching the first and second spacer material layers, leaving a portion of the first spacer material layer extending over pad of the starting structure along the sidewall of the form structure opening as recited in claim **3**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

03/12/05

Andy Huynh

Patent Examiner